BACCALAUREAT SCIENCES ET TECHNOLOGIE INDUSTRIELLES

Spécialité génie électronique

Session 2010

Etude des systèmes techniques

Option classe Européenne Italien

CARRELLO FILOGUIDATO

Carrello filoguidato

Presentazione

Il carrello filoguidato è utilizzato per assicurare una continuità nel trasporto di pezzi, tra le differenti catene di montaggio di un'impresa, con un rendimento massimo.

Il carrello è interamente automatizzato e può funzionare in modo autonomo seguendo una sequenza programmata, chiamata sceneggiatura. Segue allora un percorso predeterminato indicato da un filo di guida nascosto nel suolo.

FP4: **"INDIVIDUARE GLI OSTACOLI"**

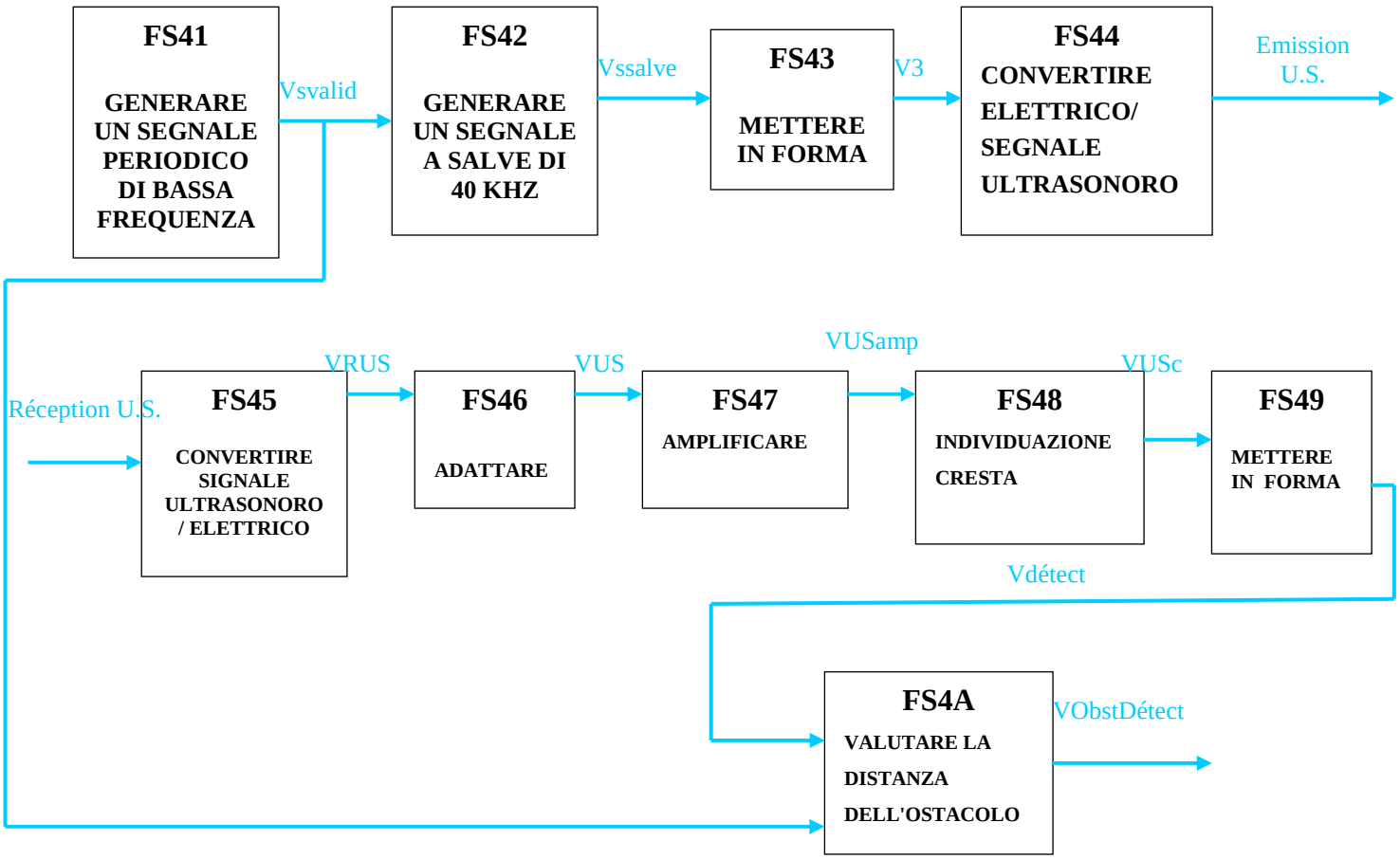
Funzione: Questa funzione permette di individuare un ostacolo presente sul percorso del carro a meno di 1 m., per evitare ogni collisione.

Questa funzione utilizza il principio della riflessione di un'onda ultrasonora in presenza di un ostacolo. FP4 genera il segnale VobstDétect che individua la presenza o l'assenza di ostacoli.

FS4A: "Valutare la distanza dell'ostacolo"

Funzione: Se l'ostacolo è localizzato a meno di 1 m dalla parte anteriore del carrello, il segnale Vdétect è convalidato. Nel caso contrario, questo non è preso in considerazione.

SCHEMA FUNZIONALE DI GRADO 2 DI FP4



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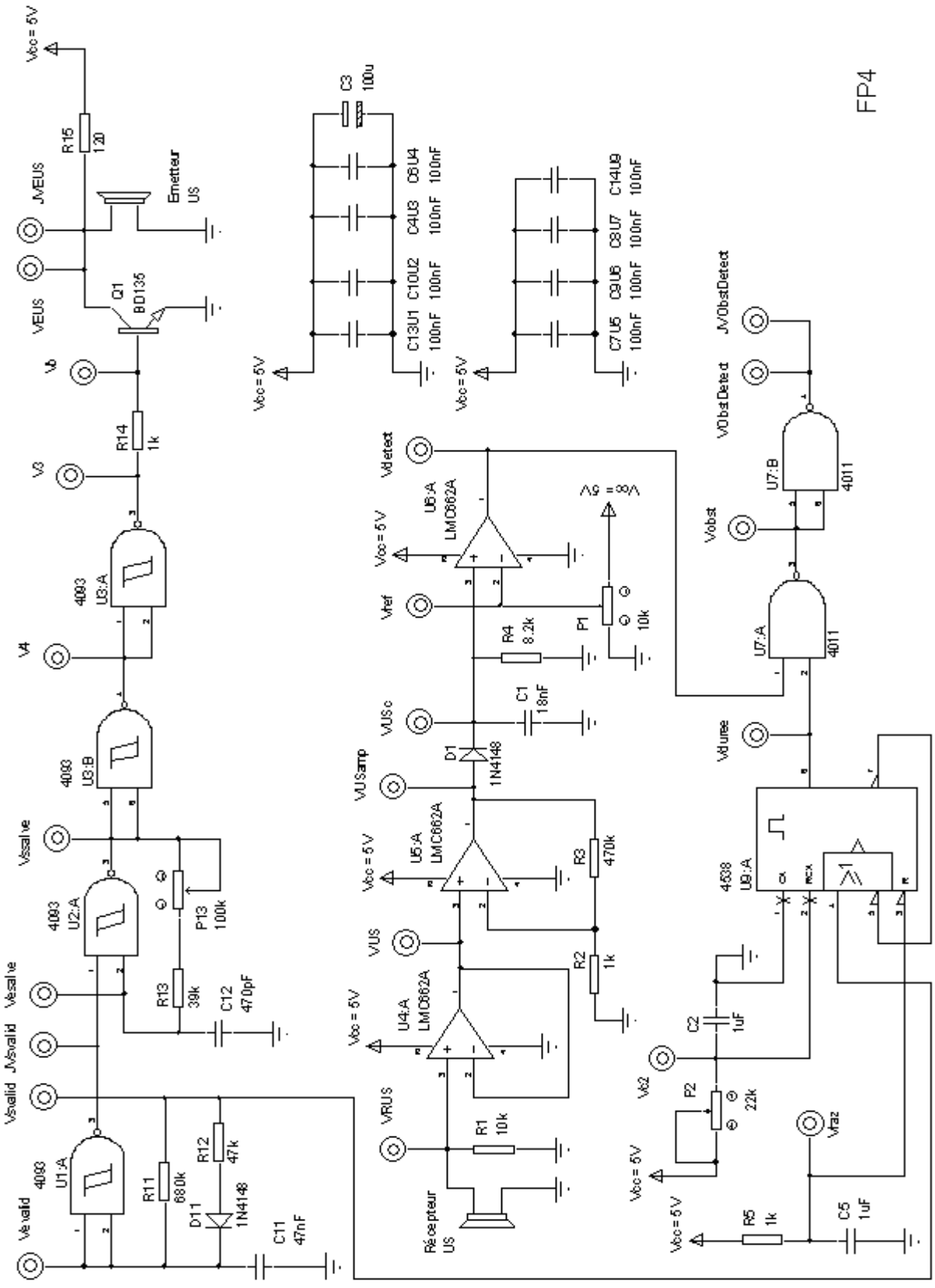
SCHEMA STRUTTURALE DI FP4



NOMENCLATURA DI FP4

Repère	Désignation du matériel	Valeur	Qté
C4,C6,C7,C8,C9,C10,C13,C14	Condensatore	100 nF, 63 V	8
C11	Condensatore	47 nF, 63 V	1
C5,C2	Condensatore	1 µF, 63 V	1
C1	Condensatore	18 nF, 63 V	1
C3	Condensatore chimico radiale	100 µF, 25 V	1
C12	Condensatore	470 pF	2
R5, R14,R2	Resistore 1/4W 5%	1 Kohms	3
R11	Resistore 1/4W 5%	680 Kohms	1
R12	Resistore 1/4W 5%	47 Kohms	1
R15	Resistore 1/2W 5%	120 ohms	1
R1	Resistore 1/4W 5%	10 Kohms	1
R3	Resistore 1/4W 5%	470 Kohms	1
R13	Resistore 1/4W 5%	39 Kohms	1
R4	Resistore 1/4W 5%	8,2 Kohms	1
P13	Potenziometro orizzontale PT10LH	100 Kohms	1
P1	Potenziometro orizzontale PT10LH	10 Kohms	1
P2	Potenziometro orizzontale PT10LH	22 Kohms	1
Q1	Transistore NPN	BD135	1
D11,D1	Diodo	1N4148	2
U1,U2,U3	CI porta NAND CMOS dip 14	CD4093	3
U7	CI porta NAND CMOS dip 14	CD4011	1
supporto U1237	Supporto CI tulipano 14 punti		4
U9	CI monostabile CMOS dip 16	CD4538	1
supporto U9	Supporto CI tulipano 16 punti		1
U4,U5,U6	CI amplificatore op dip 8	LMC662CN	3
support U456	supporto CI tulipano 8 punti		3
	Emettitore ultrasuoni diam "15mm, 40 Khz Livello di pressione del suono di KHz 120 dB		1
	Recettore ultrasuono diam "15mm, la 40 Sensibilità di KHzes - 65 dB		1
	Teste pugnale Keystone		25
J3,J4	Terminale per avvitare 3 contatti		2
JALIM	Terminale per avvitare 3 contatti		1

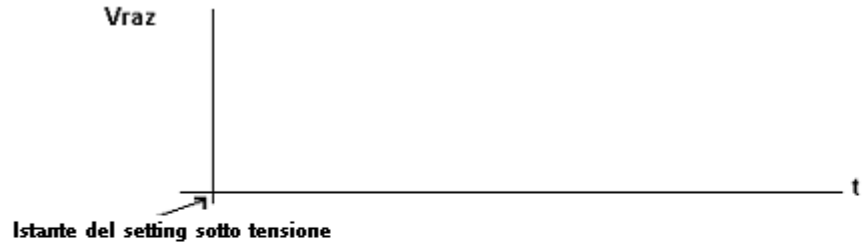
Preparazione

Segnate sullo schema strutturale le differenti funzioni secondarie.

Studio della funzione FS4.A: VALUTARE LA DISTANZA DELL'OSTACOLO:

Studio di FS42

1 Calcolate la durata Δ**t** di attivazione dell'entrata $\overline{\textbf{Reset}}$ a partire dall'istante della messa sotto tensione.



2 Nome del montaggio intorno a **U9**, e su quale segnale scatta? Doc 4538 p1.

3 Calcolate i valori estremi dell'impulso **Tw** dell'uscita Q di U9, Doc 4538 bis.

Apparecchi utilizzati: alimentatore stabilizzato.
oscilloscopio.

Misure:

Apparecchi da utilizzare: Alimentatore stabilizzato.
Multimetro (voltmetro).

Procedura di regolazione:

Collegate il montaggio a un alimentatore stabilizzato regolato a **5 V.**

Misurate con l'oscilloscopio gli stati alti e bassi di **Vdurata**., per il minimo e il massimo di **P2**.

Disegnate sul proprio foglio **Vdurata**.

Aggiustamento di **P2** per avere uno stato instabile di **6 ms.**

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2002

CD4538BC
Dual Precision Monostable

General Description

The CD4538BC is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

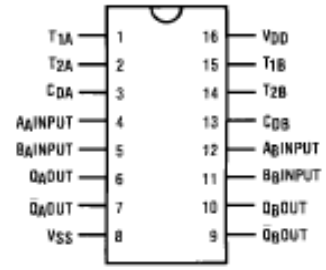
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- New formula: $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range: 1 µs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current: 5 nA (typ.) @ 5 V_{DC}
- Pin compatible to CD4528BC

Ordering Code:

Order Number	Package Number	Package Description
CD4538BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4538BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4538BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎍
H	↑	H	⎍	⎍

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎍ = One LOW Level Pulse
X = Irrelevant

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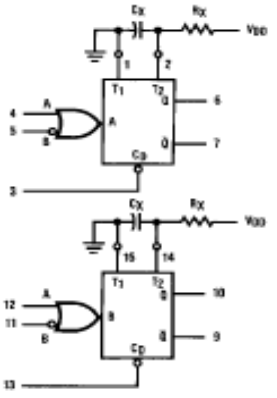
Block Diagram



R_X and C_X are External Components
V_{DD} = Pin 16
V_{SS} = Pin 8

Theory of Operation

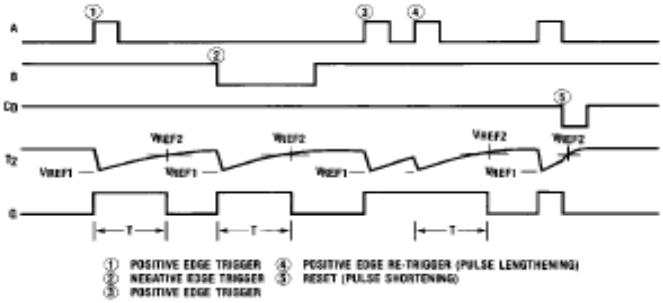


FIGURE 2.

Trigger Operation

The block diagram of the CD4538BC is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and Figure 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1[1]. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})[2].

It should be noted that in the quiescent state C_X is fully charged to V_{DD}, causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538BC is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

Retrigger Operation

The CD4538BC is retriggered if a valid trigger occurs[3] followed by another valid trigger[4] before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated[4], the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T after the last valid retrigger.

Reset Operation

The CD4538BC may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1[5]. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

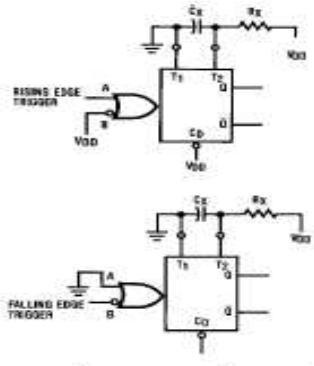


FIGURE 3. Retriggerable Monostable Circuitry

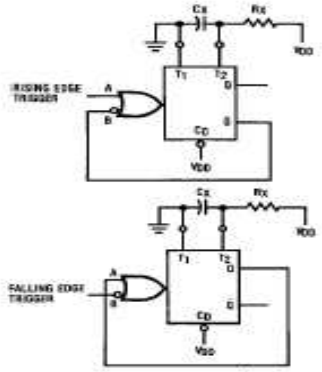


FIGURE 4. Non-Retriggerable Monostable Circuitry

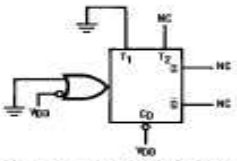


FIGURE 6. Connection of Unused Sections